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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,004	10/28/2003	Lyle E. Adams	63479.0116	4256

23309 7590 02/26/2007
Matthew J. Booth & Associates, PLLC
P O BOX 50010
AUSTIN, TX 78763-0010

EXAMINER	
DANG, KHANH	
ART UNIT	PAPER NUMBER
2111	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/695,004	ADAMS ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1639* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Application Status

Applicants filed an RCE on 1/ 18/2007 to continue prosecution of this application. Claims 1-27 were amended. New claims 28-39 were added.

Claim Rejections - 35 USC § 112

Claims 16-39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 16, line 11, "the requester" should be changed to – the requestor – to be consistent in terminology used. Further, "the requester bus protocol" and "the target bus protocol" lack antecedent basis.

In claims 20, 24, and 34, see above.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

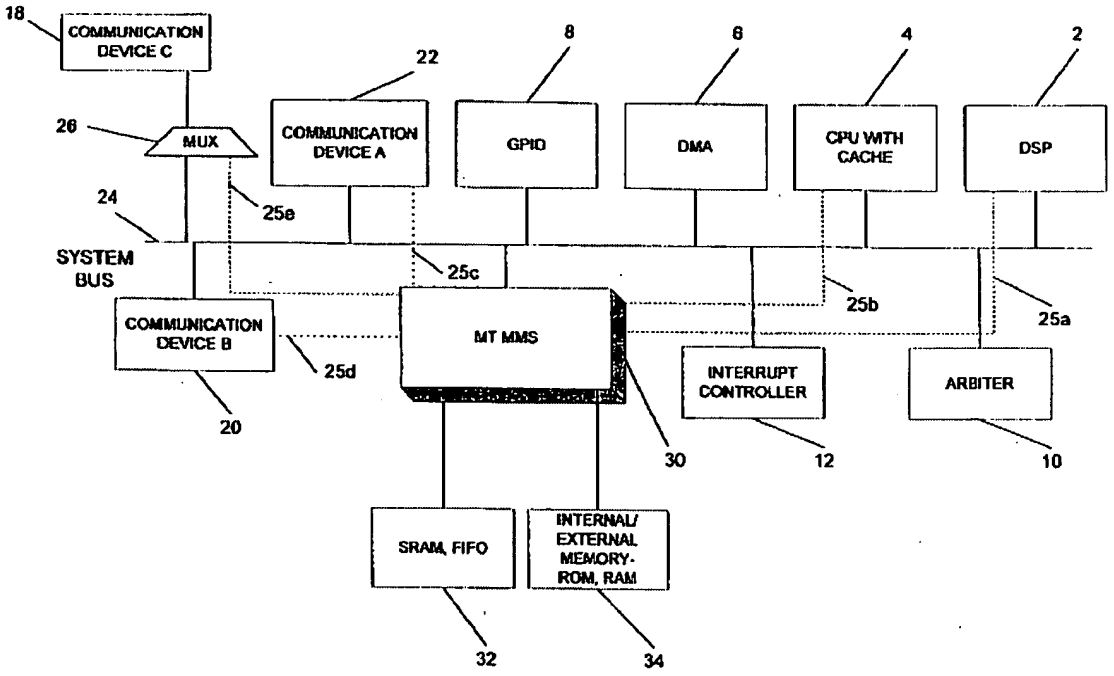
> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 16-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Elabd (6,526,462).

As broadly drafted, these claims do not define any structure/step that differs from Elabd.

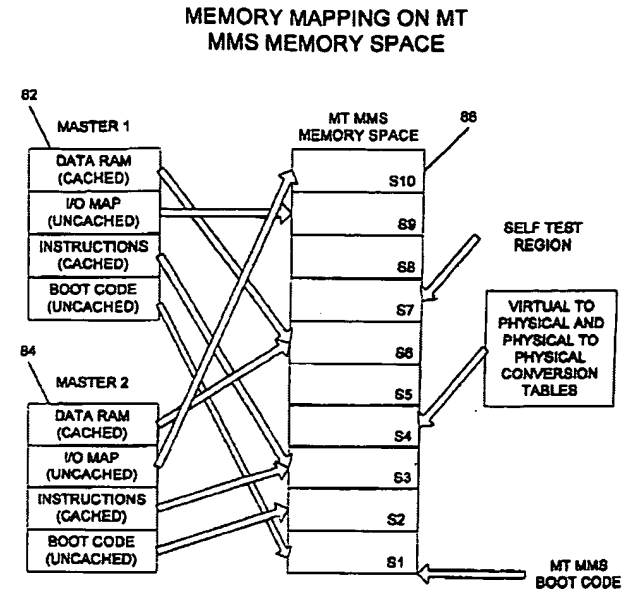
With regard to claim 16, Elabd discloses a System-on-Chip (SOC) comprising an internal switching fabric for routing signlas between requestors and addressable targets (shown generally at Fig. 2, for example, as reproduced below

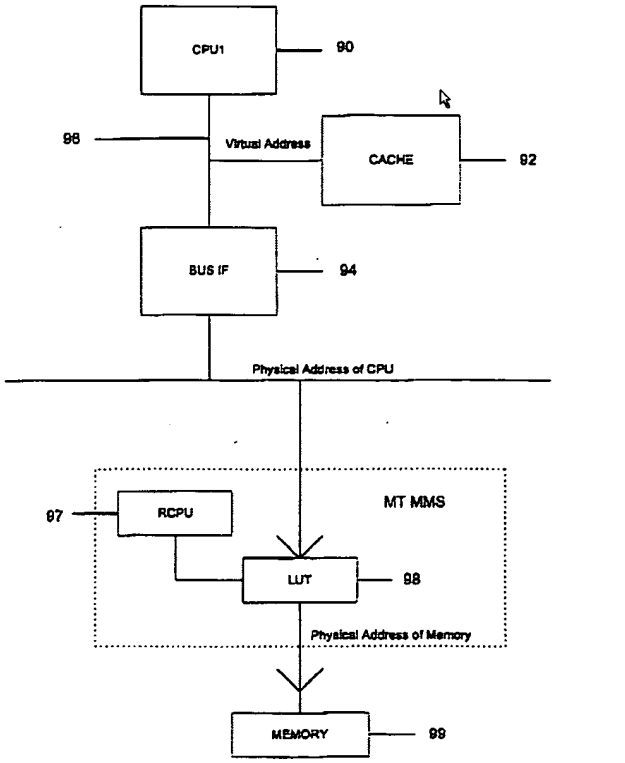
SOC USING MT MMS



,comprising: one or more connection ports coupled to one or more requestor (in Elabd, CPU 4 or DSP 2, for example, each includes at least one or more connection ports so that it can be connected to its associated devices via at least one of dedicated memory

buses 25a-25n, and MT MMS having RCPU provides communications and connections between the masters and the addressable memory targets of the memory. The MT MMS 30 is connected to the system bus 24 and various other memory masters. The MT MMS 30 receives all external memory requests from various masters and processes such requests. The memory types that are accessible using the MT MMS 30 include SRAM FIFO memory 32 or internal/external memory 34 such as ROM or RAM. Other memories such as VC-SDRAM, Flash SDRAM, and the like can also be accessible using the MT MMS 30); one or more target connection ports that couple to one or more addressable target a unique address space (the MT MMS 30 can be software configured to provide the optimal performance for the SOC product. For example, parameters are configurable by writing various configuration registers such as parity check enable/disable and memory region write protect. Beginning and ending addresses of memory banks can further be configured using software, so as to translate virtual addresses to new physical addresses. This provides a configurable memory map per each ASIC that includes the MT-MMS 30. Also, when the number of masters is changed, the memory map can be modified accordingly. Figs. 6A and 6B, which are reproduced below, illustrate examples of memory mapping on the MT MMS memory. See also col. 11, line 35 to col. 12, line 7, and Fig. 4 and description thereof.


MEMORY MAPPING ON MT MMS MEMORY SPACE
82
MASTER 1
DATA RAM (CACHED)
I/O MAP (UNCACHED)
INSTRUCTIONS (CACHED)
BOOT CODE (UNCACHED)
84
MASTER 2
DATA RAM (CACHED)
I/O MAP (UNCACHED)
INSTRUCTIONS (CACHED)
BOOT CODE (UNCACHED)
MT MMS MEMORY SPACE
86
S10
S9
S8
S7
S6
S5
S4
S3
S2
S1
SELF TEST REGION
VIRTUAL TO PHYSICAL AND PHYSICAL TO PHYSICAL CONVERSION TABLES
MT MMS BOOT CODE


CPU1
90
96
Virtual Address
CACHE
92
BUS IF
94
Physical Address of CPU
MT MMS
97
RCPU
LUT
98
Physical Address of Memory
MEMORY
99

;and one or more decoder/router elements that couple to said requestor connection ports and said target connection ports (as shown in Fig. 2 above, for example, the MT MMS 30/30A comprising routing/switching RCPU and with dedicated buses 25a-n, defines "one or more decoder/router" of an internal switching fabric of a SOC, connected between the requestor ports and target ports), each said decoder/router element receives a request from a single said requestor in the requestor bus protocol (note that as claimed, "one or more decoder router elements" is required. The phrase "each said decoder/router element" does not necessarily means – each of said decoder/router elements --. In any event, each dedicated bus 25 connected to the MT MMS 30/30A comprising routing/switching RCPU, defines each of a plurality of decoder/router elements. With regard to the phrase "the requester bus protocol, at the outset, it is noted that the "requester bus protocol" and the "target bus protocol" are different protocols. Therefore, it can be understood that the "requester bus protocol" and "the target bus protocol" can be either same protocol or different protocols. In any event, it is also noted that the MP MMS 30/30A can be configured to interface and accepts a plurality of requests from a plurality of requestors operating in different protocols such as a protocol for the CPU, protocol for the DSP, protocols for USB, Bluetooth, AC97, and different network protocols. See at least Figs. 8-10 and description thereof), determines which said addressable target is the designated target using an internal system memory map (the MT MMS 30 can be software configured to provide the optimal performance for the SOC product. For example, parameters are configurable by writing various configuration registers such as parity check enable/disable and

memory region write protect. Beginning and ending addresses of memory banks can further be configured using software, so as to translate virtual addresses to new physical addresses. This provides a configurable memory map per each ASIC that includes the MT-MMS 30. Also, when the number of masters is changed, the memory map can be modified accordingly. Figs. 6A and 6B, which are reproduced below, illustrate examples of memory mapping on the MT MMS memory. See also col. 11, line 35 to col. 12, line 7, and Fig. 4 and description thereof), and routes said request to said designated target in the target bus control protocol, wherein each said decoder/router element is coupled to said single requestor through a single said requestor port (it is clear from discussion above one or more requests from one or more requestors operating in one or more protocols is routed by the MT MMS 30/30A with dedicated buses to a designated addressable target in target memory control protocol. Further, it is also clear from discussion above that each decoder/router element is dedicatedly coupled to dedicated port of each requestor).

With regard to claim 17, it is clear that the internal switching fabric includes at least the arbiter 52 for arbitrating requests between the requestors and targets. See at least column 8, lines 15-37.

With regard to claim 18, as discussed above, it is clear that independently accessible requestor port and an independently accessible target port are provided in Elabd for a plurality of individual masters and individual targets.

With regard to claim 19, see discussion above. See also Figs. 4, 6 (a,b) and 12C, and description thereof. Note that MT MMS has the state machines. The MT MMS 30

can provide a configurable number of pipeline stages using SRAM FIFO. This can be either fixed as an RTL parameter or programmed by software. Other parameters that are configurable using the MT MMS of the present invention include configurable mask register that determines which bank stores a particular physical address issued by the master, a configurable bus width for each memory subsystem (e.g., 8, 16, 32, 64 . . . , 1024, 2048 bits), a configurable burst request register, a configurable mode registers for linear and interleaved read, and a configurable cache line read policy per master (e.g., critical word first and zero word first). The MT MMS 30 also supports dynamic programming of mode register in SDRAM (e.g., CAS latency for the SDRAM can be programmed), and provides an integrated micro-controller/CPU that provides programmable self test and system validation stimuli for multi-master transactions, as required in a complex SOC having multiple masters.

With regard to claims 20-27, see discussion above, since the subject matter presented in claims 20-27 has already been addressed.

With regard to new claim 28, it is clear from discussion above that Elabd discloses one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, and an addressable bridge to a sub-system.

With regard to new claim 29, it is clear from discussion above that one of said one or more decoder/router elements of Elabd comprises one of the following: a decoder/router element that routes requests to all of said one or more addressable targets using an internal system memory map that includes unique address space

information for all of said one or more addressable targets; a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets; or a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for less than all of said one or more addressable targets (see discussion above. Figs. 4, 6(a,b), and description thereof, and at least col. 11, line 35 to col. 12, line 7). It is also clear from discussion above that the MT MMS comprising routing/switching RCPU, and with dedicated memory buses 25a-25n, constitutes an internal switching fabric that routes signals between one or more requestors and one or more addressable targets.

With regard to new claim 30, it is clear from discussion above that Elabd discloses one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, and an addressable bridge to a sub-system.

With regard to claim 31, it is clear from discussion above that one of said one or more decoder/router elements of Elabd comprises one of the following: a decoder/router element that routes requests to all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets; a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of

said one or more addressable targets; or a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for less than all of said one or more addressable targets (see discussion above. Figs. 4, 6(a,b), and description thereof, and at least col. 11, line 35 to col. 12, line 7). It is also clear from discussion above that the MT MMS comprising routing/switching RCPU, and with dedicated memory buses 25a-25n, constitutes an internal switching fabric that routes signals between one or more requestors and one or more addressable targets.

With regard to claim 32, it is clear from discussion above that Elabd discloses one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, and an addressable bridge to a sub-system.

With regard to claim 33, it is clear from discussion above that one of said one or more decoder/router elements of Elabd comprises one of the following: a decoder/router element that routes requests to all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets; a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets; or a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for less than all of said

one or more addressable targets (see discussion above. Figs. 4, 6(a,b), and description thereof, and at least col. 11, line 35 to col. 12, line 7). It is also clear from discussion above that the MT MMS comprising routing/switching RCPU, and with dedicated memory buses 25a-25n, constitutes an internal switching fabric that routes signals between one or more requestors and one or more addressable targets.

With regard to claims 34-39, see discussion above, since the subject matter presented in claims 34-39 has already been addressed.

Response to Arguments

Applicants' arguments filed 1/18/2007 have been fully considered but are moot in view of the above discussion.

Further, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997)*. In fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.*, 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986). In addition, the fact that Elabd discloses more than what is claimed is irrelevant.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Dang whose telephone number is 571-272-3626. The examiner can normally be reached on Monday-Friday from 9:AM to 5:PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart, can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Khanh Dang
Primary Examiner